Am79R79 Ringing SLIC Device Call Processing Considerations

AMD

Application Note

A telephone line, with its connected telephones and ringers, presents a significant reactive load to the line circuit driving that line. As the telephone line circuit changes states during call processing, the SLIC device must charge and discharge these reactive loads. Because the current necessary to charge the load can be greater than detect thresholds, false detects during call processing can be generated during the changes of the SLIC states. To provide maximum application flexibility, the Am79R79 RSLIC device has no filtering on the detect output; therefore, the controlling software must provide the necessary debouncing of false detects. During typical call processing, proper use and understanding of SLIC state changes minimizes false detects.

CALL PROCESSING

During a phone call, the system controlling the telephone line changes call processing states (call states) similar to those shown in Figure 1. The SLIC must also change its states to support the system call states. The SLIC states corresponding to the call states vary based on the application. The SLIC states recommended in this document are not meant to exclude other states that are indicated for particular applications.

A typical call processing sequence is shown in Figure 1. The Service Denied call state turns off all power applied to the phone line. No communication can occur on this telephone line until this state is exited as directed by the system. As shown in this figure, the Service Denied state is entered from the Idle state, but it is possible that if service were denied in the middle of a call, then the Service Denied call state can be entered from any of the other call states.

Upon leaving the Service Denied call state, the call goes to the Idle state until there is an incoming (Call Terminating) or outgoing (Call Originating) state. (The references described here are with respect to the telephone user. An incoming call is one that rings the phone that is used to terminate the call. An outgoing call is one in which the user places a call from the telephone.)

If there is an incoming call, the system initiates the Ringing Cadence state, remaining in this state until either the phone goes off-hook and the Voice/Data Transmission call state is entered, or the originating phone goes back on-hook and the No Answer path is taken back to the Idle call state. When the Voice/Data Transmission call state is entered, the system remains in that state until the phone goes on-hook and the Idle call state is entered.

This document contains information on a product under development at Advanced Micro Devices. The information is intended to help you evaluate this product. AMD reserves the right to change or discontinue work on this proposed product without notice.

Publication# **21781** Rev: **A** Amendment: **/0**
Issue Date: **September 1997**

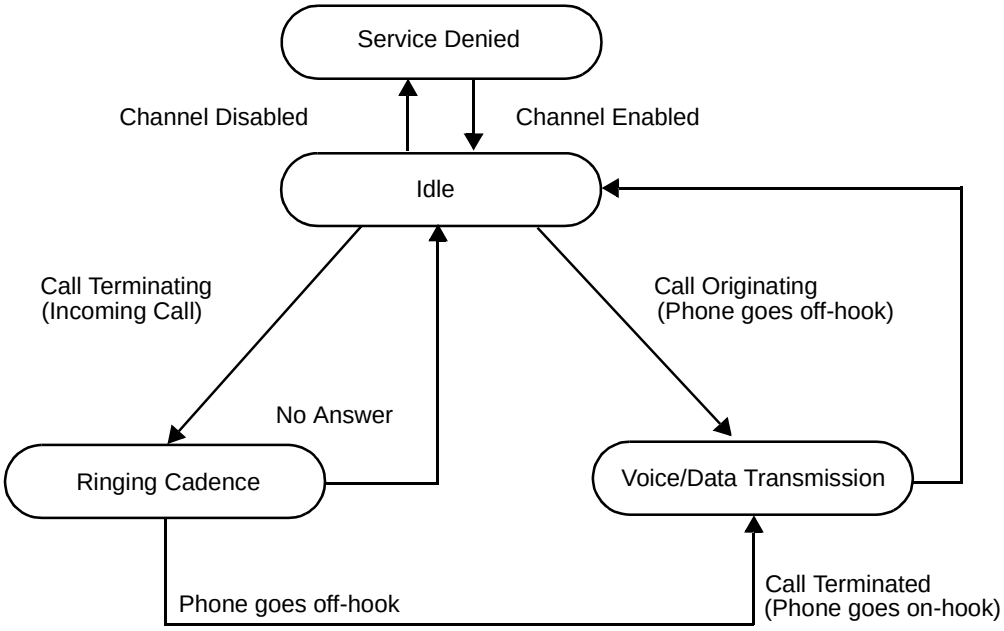


Figure 1. Typical Call Processing

SLIC STATES

A call state can require a sequence of SLIC states, such as the ringing cadence, or it can be implemented with several possible SLIC states. By choosing the most appropriate SLIC states with the appropriate battery voltage, you can save power and minimize false detects.

Idle Call State

The Idle call state can use the Active V_{BAT} SLIC state or the lower power Standby state. The SLIC exits the Idle state under two circumstances: when the phone receives a call, the system controller takes the Call Terminating path; or when the telephone is off-hook to originate a call, the system controller takes the Call Originating path.

Ringing Cadence State

The Call Terminating branch leads to the Ringing Cadence call state, requiring the telephone to ring to get the subscriber's attention. The ringing cadence can be generated with timings that vary depending on the country involved. Regardless of timing, the ringing cadence alternates between a ringing and a quiet period.

The ringing cadence is a transition from the SLIC state for Ringing to a quiet state using one of three SLIC states—Standby, OHT, or Active. The Standby SLIC state does not allow on-hook transmission used for caller ID; therefore, choose either the OHT or Active SLIC state to support caller ID. The OHT SLIC state has a small power savings (20–50 mW) over the Active SLIC state. The two states act the same with respect to false detects and support on-hook transmission, so they are interchangeable for the Ringing Cadence state. The ringing cadence chosen is from the Ringing SLIC state switching to the Active SLIC state, repeated with the appropriate timing for a specific application.

To generate enough voltage to ring the telephone, select V_{BAT1} during the Ringing SLIC state. Make sure that there is enough Tip-Ring voltage so that devices on the telephone line recognize a call in process; use V_{BAT1} with the Active SLIC state. To minimize the false detect duration during cadencing, keep the ringing voltage as close to the Active state voltage as possible. The Tip-Ring voltage is controlled by the voltage on RINGIN input. The RINGIN input is the waveshaped version of the ringing input signal that is applied to R_{SLEW}. When this input is High, the A lead is driven toward ground and the B lead is driven toward V_{BAT1}. The ringing signal and the load take time to settle. Therefore, synchronize the switch from Ringing to Active state to the end of the RINGIN High or immediately after it switches Low. This switch minimizes the false detect duration.

When a phone goes off-hook during ringing cadencing, the call proceeds to the Voice/Data Transmission call state. If the phone does not go off-hook before the originating caller puts the phone on-hook, the call state returns to the Idle state.

Voice/Data Transmission

The Voice/Data Transmission call state can be entered from the Idle state if the phone goes off-hook to initiate an outgoing call, and from the Ringing Cadence state if there is an incoming call. In either case, the phone is off-hook to either answer or originate a call when in the Voice/Data Transmission call state. The Voice/Data Transmission call state uses the Active SLIC state with V_{BAT2} to save power—you can use V_{BAT1} but it uses more power. When the call ends by the phone going back on-hook, the SLIC returns to the Idle state by means of a transition from Active V_{BAT2} to Active V_{BAT1} or Standby SLIC States. The state transitions listed in Table 1 are for a typical system.

Table 1. Possible State Transitions in a SLIC for Call Processing in Figure 1

Call State Transition	SLIC State Transitions	Reason for Transition
Service denied to or from Idle	Open Circuit to Standby and vice-versa	System decision to deny or grant service
Idle to Ringing Cadence	Standby to Ringing Cadence	Initiate ringing for incoming call
Ringing Cadence	Ringing to Active V_{BAT1} and vice-versa	Perform ringing function
Ringing Cadence to Idle	Ringing or Active V_{BAT1} to Standby	No off-hook occurred before the call originator went on-hook
Ringing Cadence to Voice/Data Transmission	Ringing or Active V_{BAT1} to Active V_{BAT2}	Phone went off-hook and the call state went to Voice/Data Transmission
Idle to Voice/Data Transmission	Standby to Active V_{BAT2}	Phone went off-hook to initiate call
Voice/Data Transmission to Idle	Active V_{BAT2} to Standby	Phone went on-hook to end call

SLIC STATE TRANSITIONS AND FALSE DETECTS

The false detects that occur during a SLIC state transition arise as a consequence of the nature of the telephone line impedance, which can range from an open circuit to an RLC network. The load used depends on the service provided and the country in which the part is applied.

This note focuses on the loads in the United States, because the U.S. 5REN load is the largest. The considerations are similar for other countries and for small loads, the false detects are shorter.

When using different versions of the 5REN model, you get different results. Figure 2 shows the two versions of the 5REN mode. The first is an RLC network consisting of 730 Ω in series with 22 H in series with 2.25 µF. The second is an RC network consisting of 40 µF in series with 1386 Ω. The time constant for the circuit in Figure 2b is 55.4 ms. The false detect duration is dependent upon the load and the voltage change; fewer REN loads or less change in voltage creates shorter duration false detects.

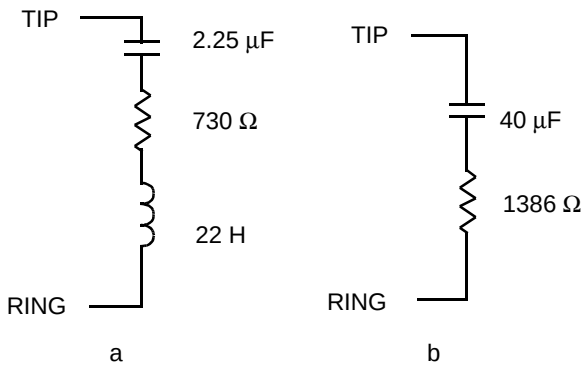


Figure 2. Two Models of 5REN Loads

The external components used with the Am79R79 RSLIC device affect the duration of false detects. The loop current limit affects the charging time of the load: an increased current decreases the charging time. The ringing current is usually high enough that changing it does not decrease the false detect durations. During state changes, the time constant of the current limit network for loop current (R_{DC1}, R_{DC2}, C_{DC}) and ringing current (R_{DCR1}, R_{DCR2}, C_{DCR}) affects the state transitions. To keep the effect of these time constants to a minimum, use the minimum values: 15 µs for the ringing time constant and 2 ms for the DC loop time constant.

Any change in voltage across the load can cause transient currents to flow. If the transient current is above the detect threshold, there is a false detect. The state transitions in Table 1 are typically used and their usual false detect durations are examined. In most cases, this is attributable to the load and is unavoidable. During SLIC state changes with an open circuit load, there may be some short duration false detects, typically less than a few milliseconds but not more than 10 ms, which your system should debounce.

Figure 3 shows the Am79R79 loop detect circuitry. The loop current is scaled and output to the RD pin, where the current creates a voltage across RD. This voltage is compared to BREF, which is dependent upon the state of B2EN, the voltage from tip to ring (V_{AB}), and the SLIC state as outlined in the *Am79R79 Ringing SLIC Technical Overview Application Note* (PID# 19768B). For the Active and OHT states, a scaled value of V_{AB} appears at BREF. The scaled value allows the Am79R79 RSLIC device to detect at a loop resistance rather than a current, eliminating problems with battery variation influencing loop detect thresholds. The exact scale value is dependent upon which battery is selected. When the SLIC is in the Standby state, a constant voltage is applied at BREF. When in all SLIC states but Ringing and Disconnect, the $\overline{DET}$ output is connected to the output of the loop detect comparator shown in Figure 3. There is no filtering from I_{LOOP} to Loop Detect, so any variations in the loop current can cause an instantaneous change in the $\overline{DET}$ output.

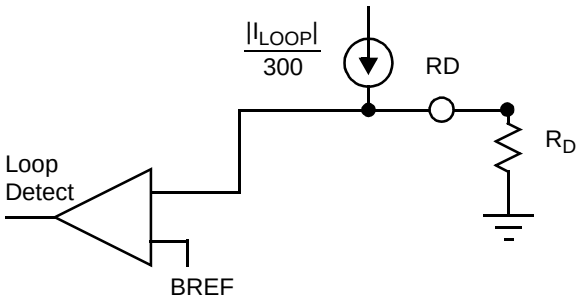


Figure 3. Loop Detect Circuitry

STATE TRANSITIONS WITH INSIGNIFICANT FALSE DETECTS

A state changes when a large reactive load is on the loop; state transition false detects occur because the phone is on-hook. The transient current needed to charge the load to the appropriate voltage can cause a false detect on the DC loop detect pin.

If the phone is off-hook before the state transition occurs, there is no significant false detect. This happens in several SLIC state changes, which are not discussed in this document: the transition from Idle to

Voice/Data Transmission (Standby or Active V_{BAT1} to Active V_{BAT2}), and the transition from Ringing Cadence to Voice/Data Transmission (Ringing or Active V_{BAT1} to Active V_{BAT2}). These transitions can have false detects of less than 10 ms, which are not significant. Table 2 lists the state transitions that cause significant $\overline{DET}$ false detect.

Table 2. State Changes Causing $\overline{DET}$ False Detect

State Changes
Open Circuit to Standby
Standby to Ringing
Standby to Active V_{BAT1}
Active V_{BAT1} to Ringing
Ringing to Active V_{BAT1}
Active V_{BAT1} to Standby
Ringing to Standby
Active V_{BAT2} to Standby
Active V_{BAT2} to Active V_{BAT1}
Standby to Active V_{BAT2}
Ringing to Active V_{BAT2}
Polarity Reversal

When service is denied to a channel, ignore any false detects, so that the Standby to Open Circuit case is not examined. The Active V_{BAT2} Polarity Reversal only occurs in Off-Hook state and generates a short duration false detect (less than 5 ms) during the time the tip and ring voltages are nearly equal during the polarity reversal time.

FALSE DETECT DURATION AND SOURCES

The following states discussed are SLIC states.

Open Circuit–Standby

When in open circuit, the load is completely discharged because there is no voltage applied. The Standby state charges the load to V_{BAT1} –10 V. The Tip and Ring are connected to ground and V_{BAT1}, respectively, through 200 Ω each, but the switches that connect the resistors have a current limit which can be below 20 mA (see the *Am79R79 Data Sheet*). The $\overline{DET}$ false detect is less than 100 ms. This occurs when service is being granted to the channel and can be masked easily by the system.

Standby–Ringing

There is little or no false detect if the Ringing state is entered from Standby at the time shown in Figure 4. This moment occurs when RINGIN has been High for one-half of a ringing period and the load has had time to settle. Ringing state can also be entered just after the High-to-Low RINGIN transition occurs because the voltage at Tip and Ring does not change instantaneously. A false detect can occur if Ringing state is entered towards the end of the time period that RINGIN is low, which has the A and B leads in the opposite polarity that it enters Standby. This polarity reversal causes a large ringing current to charge the load and change the opposite polarity. The length of the $\overline{DET}$ false detect is dependent upon the ringing current limit that the application requires. With a 100 mA current limit, it should be less than 20 ms; a lower current limit takes proportionately more time.

Standby–Active V_{BAT1} and Active V_{BAT1}–Standby

This transition produces very little false detect. Active V_{BAT1} and Standby have a similar open circuit voltage so the current level that the load requires to charge is small. If there is a $\overline{DET}$ false detect, it is only a few milliseconds.

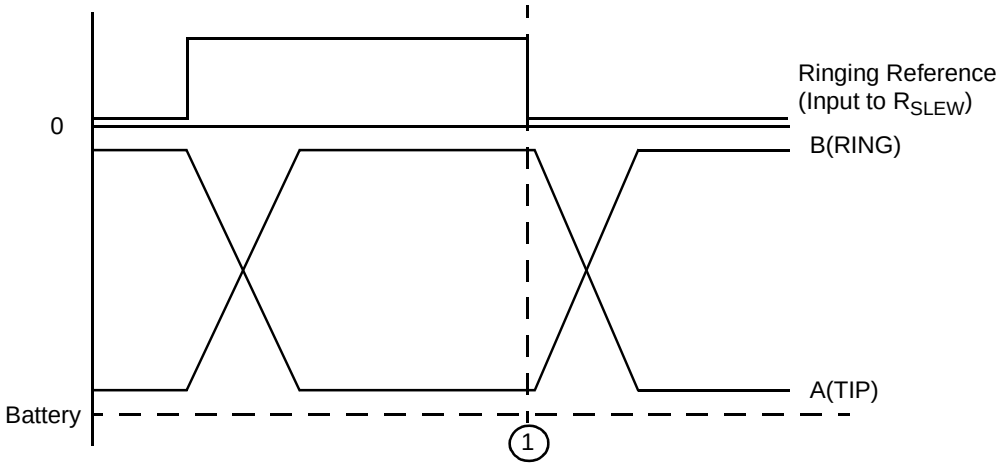
Active V_{BAT1}–Ringing

Like the Standby–Ringing transition, synchronize this transition with RINGIN high to give a minimum false detect state change. You do not have to wait until the end of the RINGIN High period. The Active state charges the load to the appropriate DC voltage, so a transition from Active to Ringing at any time during RINGIN high is acceptable. The $\overline{DET}$ false detect is less than 10 ms.

Ringing–Active V_{BAT1} or Active V_{BAT2}

Synchronize this transition to the end of RINGIN High or at the time that RINGIN goes from High to Low. Even properly synchronized, this transition can have a $\overline{DET}$ false detect of about 120 ms. This is due to the charging of the load and to the DC feed of the Am79R79 RSLIC device. During ringing the voltage at RDC discharges to near-ground; the 20 ms time constant of the DC feed must charge, and during the charge time the current available to the load decreases. The Anti-saturation turn-on slows the settling while it decreases the available current to charge the load.

This transition is affected by the loop current limit; the 120 ms time assumes a 25 mA loop current limit, and the false detect duration decreases if the loop current limit increases. Figure 4 shows the relationship of RINGIN and the waveforms at TIP and RING.



1. The best time for switching between RINGING and other states to minimize detect switching transients.

Figure 4. Ringing Waveforms

Ringing–Standby

Synchronize this transition to the end of RINGIN High or at the time that RINGIN goes from High to Low. The duration is dependent on the actual current limit for the Standby state, which can be a bit less than 20 mA. The $\overline{DET}$ false detect has a duration of 60 ms or less.

Active V_{BAT2}–Standby

This transition requires that the load be charged from V_{BAT2} to V_{BAT1}–10. Depending on the values of V_{BAT2} and V_{BAT1}, there can be a significant difference in voltage and this transition can have a $\overline{DET}$ false detect up to 40 ms.

Standby–Active V_{BAT2}

This state change requires the load be discharged from V_{BAT1}–10 to V_{BAT2}. Depending on the values of V_{BAT2} and V_{BAT1}, there can be a significant difference in voltage and this transition can have a $\overline{DET}$ false detect of 100 ms.

Active V_{BAT2}–Active V_{BAT1}

This state change requires that the load be charged from the low battery voltage to the high battery voltage. With a 25 mA loop, the $\overline{DET}$ false detect takes less than 80 ms; with a higher loop current limit, the false detect time decreases.

POLARITY REVERSAL

The Polarity Reversal state transition creates a long false detect if it occurs while the phone is on hook. Several protocols can cause this. The polarity reversal causes a voltage change across the load equal to twice the open circuit voltage. A V_{BAT1} polarity reversal causes a false detect of approximately 250 ms. A V_{BAT2} polarity reversal causes a false detect of about 150 ms. Most of the false detect is caused by the loop current charging the load through the large voltage change. It is further slowed by the DC-feed time constant, which increases the time required to reverse the polarity of the feed current.

If the polarity reversal occurs while the phone is off hook, a false detect of 10 ms or less occurs as the voltage from tip to ring nears zero.

Components that Modify False Detect Duration

The length of the false detect is affected by a number of circuit elements, (assuming V_{BAT1} = 70 V, V_{BAT2} = 24 V, and the component values as shown in the application circuit in the *Am79R79 Data Sheet*) including battery voltage and loop current limit.

The battery voltage affects the duration of the false detect in the Ringing and Standby states, because the peak voltage change possible from tip to ring is dependent upon the battery voltage. The battery has little effect in anti-saturation states (Active, OHT, and Polarity Reversal). The anti-saturation voltage affects the false detect duration in these states, so use of R_{SGH} and R_{SGL} to increase or decrease the open circuit voltage increases or decreases the duration of the false detect. R_{SGH} and R_{SGL} have limited range and therefore, have limited effect on the false detect duration.

The loop current limit (25 mA typical) affects the false detect duration in all but Ringing and Standby SLIC states. Higher loop current limits decrease the duration of the false detect. The current limit is determined by

R_{DC1} and R_{DC2}; the DC-loop time constant formed by these two resistors and C_{DC} also affects the false detect duration. The amount of time necessary for the DC loop to turn on when transitioning from the Ringing state to an Active state, or during a polarity reversal, is dependent on the DC-loop time constant. To ensure stability, the data sheet specifies 19 ms. To minimize the false detect duration, design the DC-loop time constant to a minimum of 19 ms.

The loop detect threshold determined by the resistor R_D sets the level at which the detect circuitry triggers. The detect threshold can be set as outlined in the *Am79R79 Technical Overview*. By setting the detect level at a lower resistance (i.e, higher current) the duration of the false detect can be reduced.

The ringing current limit is not likely to be a factor in the length of the false detect. The current limit typically is sufficient to drive the intended load without the ringing detect threshold being triggered. In applications where a low ringing current limit is used, the REN load is also lower.

The ringing load has a major load in determining false detect length. This document assumes; if a system drives fewer REN, the false detect duration decreases.

RING TRIP

Ring trip is not a state transition but it warrants attention because the onset of ring trip is defined as the loop resistance at which the $\overline{DET}$ output begins to pulse momentarily low each ringing cycle. This definition allows detection of ring trip at the highest possible loop resistance, but it is a periodic false detect that you must debounce. Figure 5 shows the ring-trip circuitry, in which the loop current is scaled and the absolute value taken. The current is then filtered by C_{RT}, R_{RT1}, and R_{RT2} and this waveform is compared to ground. R_{RT1} connects to V_{BAT1}, which provides an offset for the ring-trip signal to overcome, helping establish the threshold. When not in Ringing state, the 15 μA current source provides a bias to the RTRIP1 node because the R_{RT1} connection to V_{BAT1} is open.

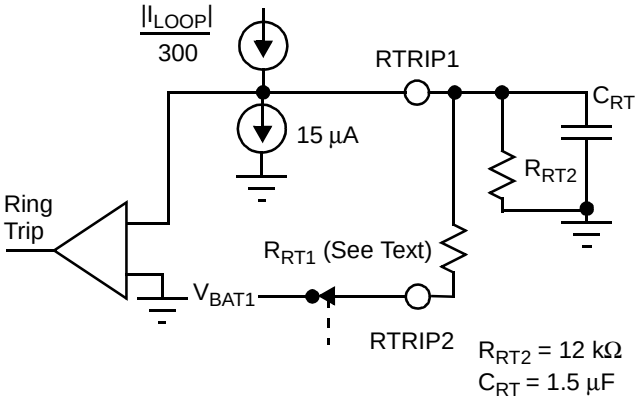


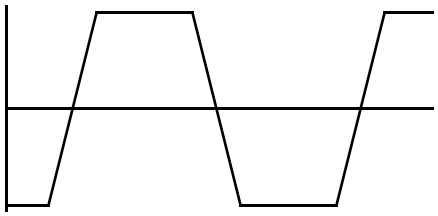
Figure 5. Ring Trip in Ringing State

Figure 6 shows sample waveforms illustrating ringing and ring trip. Figure 6a shows the loop current into a resistive load. Figure 6b shows the scaled and absolute value version of the loop current. Figure 6c shows the filtered waveform. As the loop current changes, the filtered waveform has a DC shift that changes the $\overline{DET}$ output. The three levels, A, B, and C show the effect of increasing loop current (decreasing loop resistance), which increases the DC level of the filtered waveform. In Figure 6c, the A level represents ground with respect to the filtered waveform when the loop resistance is at R_{LRT}, the ringing detect threshold resistance. B is at a lower resistance, and C is at an even lower resistance, which causes the $\overline{DET}$ output to go low steadily. Figure 6d through 6f illustrate the waveform expected from the $\overline{DET}$ pin as the DC level moves from A to C.

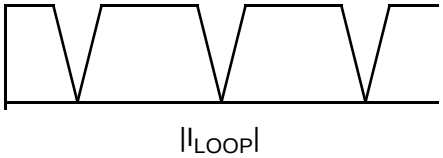
As the loop resistance decreases, the pulse width at the $\overline{DET}$ output increases until it is at a constant logic Low. The equation that defines the onset of ring trip in terms of R_{RT1} as given in the application note is:

$$R_{RT1} = 300 \bullet CF \bullet \frac{V_{BAT1}}{V_{BAT} - 3.5 - (15\ \mu A \bullet 300 \bullet CF \bullet (R_{LRT} + R_S + 2R_F))} \bullet (R_{LRT} + R_S + 2R_F)$$

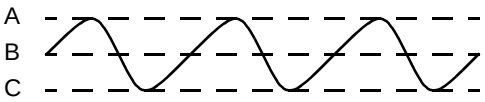
This equation shows that the ring-trip threshold resistance (R_{LRT}) is dependent on a number of parameters, including the crest factor of the ringing waveform. This equation is valid near a ringing frequency of 20 Hz. When verifying this, use a true rms meter or a digital oscilloscope that calculates rms values because an average responding meter cannot measure this accurately. The ring trip threshold is dependent on the ringing frequency, battery voltage, ring trip threshold, crest factor, and definition of ring-trip onset. Ring-trip definitions can be pulse onset as shown in Figure 6d, a 50% duty cycle as shown in Figure 6e, or a flat line as shown in Figure 6f. Figure 7 shows how ring-trip definition varies for a ringing frequency of 20 Hz, V_{BAT1} = 60 V, and RRT1 varies as shown along the x-axis.



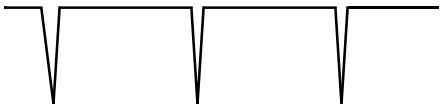
a. Ringing current flowing into a resistive load.



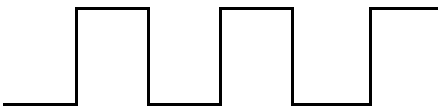
b. Current flowing from the RTRIP1 pin.



c. Filtered current. A, B, and C show various ground levels demonstrating the effect of loop current on the $\overline{DET}$ false detect.



d. This is the $\overline{DET}$ output at the onset of ring trip at the RLRT value and corresponds to the 'A' level in c.



e. $\overline{DET}$ signal for the B ground reference in c.

f. $\overline{DET}$ signal for the C ground reference in c.

Figure 6. Ring Trip Waveforms

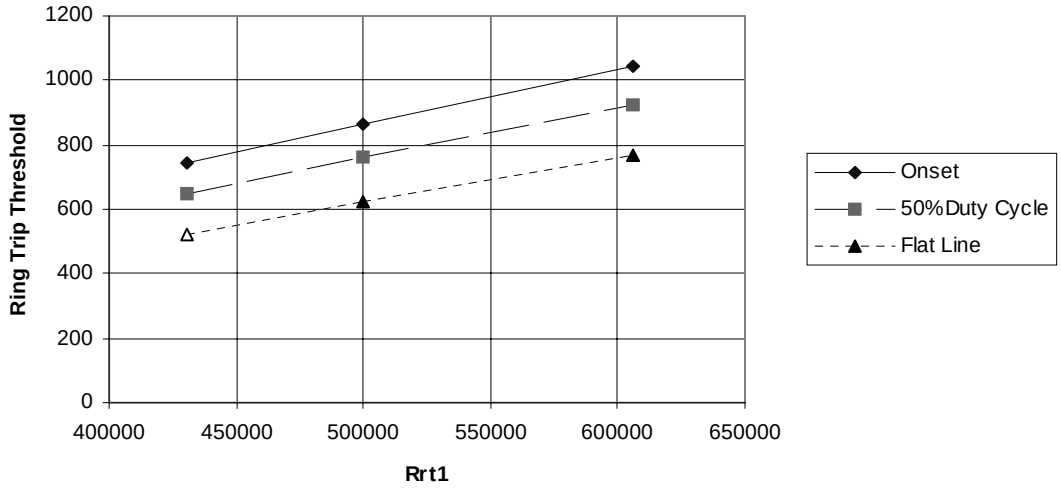


Figure 7. Ring-Trip Threshold for Onset, 50% Duty Cycle, and Flat Line

ADDITIONAL REFERENCES

Am79R79 Data Sheet, PID# 19752B

Am79R79 Ringing SLIC Technical Overview Application Note, PID# 19768B

Am79R79 Ringing SLIC User Guide Application Note, PID# 21109A

Bigelow, S., "Understanding Telephone Electronics", *Newnes,* 1997

Reeve, Whitham D., *Subscriber Loop Signaling and Transmission Handbook: Analog*, IEEE Press, 1991

Trademarks

Copyright © 1997 Advanced Micro Devices, Inc. All rights reserved.

AMD, the AMD logo and combinations thereof are trademarks of Advanced Micro Devices, Inc.

Product names used in this publication are for identification purposes only and may be trademarks of their respective companies.